ABSTRACT OF THE DISCLOSURE

A method for fabricating a single-electron transistor (SET). A one dimensional channel is formed between source and drain on a silicon-on-insulator substrate, and the separated polysilicon sidewall spacer gates are formed by electron-beam lithographically etching process in a self-aligned manner. Operation of the single-electron transistor with self-aligned polysilicon sidewall spacer gates is achieved by applying external bias to the self-aligned polysilicon sidewall spacer gates to form two potential barriers and a quantum dot capable of storage charges between the two potential barriers. A metal upper gate is finally formed and biased to induce a two-dimensional electron gas (2DEG) and control the energy level of the quantum well. Accordingly, the method of the invention comprises a combination of electron beam (E-beam) lithography with multilayer-aligned direct writing technology, oxidation, and wet etching to form a nanoscale one-dimensional channel between source and drain on a silicon-on-insulator substrate.